AMENDMENTS TO THE CLAIMS

In the Claims

Please amend the claims as follows:

1. (Currently Amended) A circuit for evaluating duration ~~and/or~~ or shape characteristics of an electric pulse induced in an element of an integrated circuit, comprising:

an assembly of elements (D1 to Dn; d1 to dn), each element being likely to receive an occasional external disturbance generating an electric pulse in the element, wherein an element is an OR gate, an AND gate, an inverter or any element in a cell library; and

a measurement circuit (B1 to Bn, 1; b1 to bn, ~~20~~) connected to the elements to determine said characteristics of an electric pulse generated in one of the elements.

2. (Currently amended) The evaluation circuit of claim 1, for an evaluation of the duration of a pulse generated in one of said elements, wherein said elements form a chain of elements (D1 to Dn) in series to propagate a pulse generated in one element through the next elements, the measurement circuit comprising:

storage means (B1 to Bn) for storing at a given time ~~the~~ output levels of the elements; and

a determination means ~~(1; 4)~~ for determining, based on the storage means, ~~the~~ a number of elements indicating levels distinct from ~~the~~ an idle level.

3. (Currently amended) The evaluation device of claim 2, wherein the determination means indicate a duration equal to the number of elements indicating levels distinct from the idle level multi-plied by ~~the~~ a propagation time through an element.

4. (Currently amended) The evaluation circuit of claim 2, wherein the storage means are formed of flip-flops (B1 to Bn) controlled by a same clock signal (CLK), ~~the~~ an output of each circuit element (Di) being connected to ~~the~~ a data input of a flip-flop (Bi), ~~the~~ a data output of each flip-flop being connected to the determination means.

5. (Currently amended) The evaluation circuit of claim 2, wherein the storage means are formed of flip-flops (B1 to Bn) in series controlled by a same clock signal (CLK) and of several ~~multi-plexers~~ multiplexers (M1 to Mn), ~~the~~ an output of a flip-flop (Bi) being

connected to a first input of a multiplexer (Mi) having its output connected to ~~the~~ a data input of the next flip-flop (Bi+1), ~~the~~ a second ~~inputs~~ input of the multiplexers receiving the outputs of the circuit elements (D1 to Dn), the data output of the last flip-flop (Bn) being connected to the determination means.

6. (Currently amended) The evaluation device of claim 5, further comprising a detector circuit ~~(5)~~ indicating whether no flip-flop, a single one, or several ones have switched, and wherein the data output of the last flip-flop (Bn) is connected to a counter ~~(4)~~ which counts ~~the~~ a number of successive flip-flops~~, the~~ stored levels of which are distinct from the idle levels, the counter receiving the stored levels in series when the multiplexers (M1 to Mn) are set to have the stored levels pass from one flip-flop to another at the rate of the clock signal (CLK).

7. (Currently amended) The evaluation circuit of claim 6, further comprising a control circuit ~~(6)~~ which:

initially sets the multiplexers (M1 to Mn) in a capture mode by connecting the outputs of the circuit elements (D1 to Dn) to the data inputs of the flip-flops (B1 to Bn);

sets the multiplexers in a counting mode to have the stored levels pass from one flip-flop to another when the detector circuit indicates that at least two flip-flops have switched state, and

resets the multiplexers in capture mode when the counter indicates ~~the~~ an end of the counting.

8. (Currently amended) The evaluation circuit of claim 7, wherein the circuit elements (D1 to Dn) are non-inverting circuits and the flip-flops (B1 to Bn) are set to level "0", and wherein the detector circuit ~~(5)~~ comprises two first OR gates ~~(10, 11)~~, each first OR gate receiving one flip-flop data output out of two, the outputs of the first two OR gates entering a second OR gate ~~(12)~~ and an AND gate ~~(13)~~, the control circuit receiving ~~the~~ outputs of the second OR gate and of the AND gate.

9. (Currently amended) The evaluation circuit of claim 7, wherein the circuit elements (D1 to Dn) are inverter circuits and the flip-flops (B1 to Bn) are set, half to level "0" and half to level "1", and the detector circuit ~~(5)~~ comprises a first OR gate receiving the outputs of the flip-flops set to "0", and a first AND gate receiving the outputs of the flip-flops set to "1", ~~the~~ outputs of the first two gates entering a second OR gate ~~(12)~~ and a second AND gate ~~(13)~~, the control circuit receiving ~~the~~ outputs of the second OR gate and of the second AND gate.

10. (Currently amended) The circuit of claim 2, wherein the storage means are formed of groups of flip-flops (B1 to Bn) controlled by a same clock signal, each group of flip-flops receiving ~~the~~ outputs of groups of circuit elements, ~~the~~ a number of flip-flops being smaller than the number of circuit elements, ~~the~~ and data output of each flip-flop being connected to the determination means ~~(20)~~.

11. (Currently amended) The circuit of claim 1, for evaluating the shape of a pulse generated in one of said elements, wherein the elements are controlled so that a transistor having a drain and a source (T1 to Tn) comprised in each element is non-conductive, the drain or the source of a non-conductive transistor of each element being connected to a common node (N), the measurement circuit ~~measur-ing~~ measuring ~~the~~ variations of the common node voltage when an external disturbance hits the drain or the source of a transistor connected to the common node.

12. (Currently amended) The circuit of claim 11, comprising an amplifier ~~(40)~~ of the common node voltage (N) and several analog flip-flops (b1 to bn) capable of storing ~~the~~ an output voltage level of the amplifier, the flip-flops being controlled by an assembly of clocks (Ck1 to Ckj) offset with respect to one another.

13. (Currently amended) The circuit of claim 11, comprising an analog-to-digital converter ~~(60)~~ of the voltage at the common node (N) providing a digital value of the voltage over n bits (Bit1, Bit2, Bit3), and several groups of binary flip-flops (g1 to gj), each group of flip-flops comprising n flip-flops each capable of storing the value of one of the n bits, the groups being controlled by an assembly of clocks (Ck1 to Ckj) offset with respect to one another.

14. (Currently amended) The circuit of claim 11, comprising a load circuit ~~(30)~~ capable of setting to order the common node (N) to a given voltage.

15. (Originally submitted) The circuit of claim 11, wherein each transistor is connected to the common node by a connection, the connections being of same lengths.

16. (Originally submitted) The circuit of claim 12, wherein the offset clocks (Ck1 to Ckj) are provided by a circuit comprising several chains of delay elements (s1, s2) each receiving a clock signal,

the first delay elements (s1-1, s2-1) of each of the chains introducing different delays (DEL1, DEL2), the outputs of each of the elements of said chains providing said clocks.

17. (Currently amended) A method for evaluating duration ~~and/or~~ or shape characteristics of an electric pulse induced in an integrated circuit element, comprising the steps of:

forming a circuit comprising a ~~great number~~ plurality of elements, each element being likely to receive an occasional external disturbance generating an electric pulse in the element; wherein an element is an OR gate, an AND gate, an inverter or any element in a cell library; and

determining, by means of a measurement device connected to the elements, said characteristics of an electric pulse generated in one of the elements.

18. (Currently amended) The method of claim 17 comprising evaluating the duration of a pulse generated in one of said elements, wherein the step of forming a circuit comprises arranging a ~~great number~~ plurality of circuit elements (D1 to Dn) in series in an idle state, each circuit element being connected to propagate to the next circuit element a pulse provided by ~~the~~ an immediately preceding circuit element, and wherein the determination step comprises periodically storing in storage means ~~the~~ an output level of each circuit element and of determining ~~the~~ a number of storage means indicating levels distinct from the idle level.

19. (Currently amended) The method of claim 17 comprising evaluating the shape of a pulse generated in one of said elements, wherein the circuit elements are controlled so that a transistor of each element is non-conductive, the transistor having a drain and a source, and the drain or the source of a non-conductive transistor of each element being connected to a common node, and wherein the determination step comprises measuring ~~the~~ variations of the common node voltage when an external disturbance hits the drain or the source of a ~~transis-tor~~ transistor connected to the common node.